Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of claims:

1. (Currently amended) A method for remapping locations in memory, comprising:

generating a remapping value by logically combining a bad address value with an unused address value;

logically combining the remapping value with an intended address value to generate a remapped address value, wherein one or more bad memory address values exist and wherein the remapping value is logically combined with only intended address values that equal one of the bad memory address values to generate a remapped address value for only the one or more bad memory address values; and

accessing a memory location having the remapped address value.

2. (Cancelled)

3. (Currently amended) The method of claim ~~2~~1, wherein the bad memory address value, unused memory address value, and the remapped address value correspond to individual data locations.

4. (Currently amended) The method of claim ~~2~~1, wherein the bad memory address value and the unused memory address value each correspond to multiple data locations.

5. (Currently amended) The method of claim ~~2~~1, wherein the bad memory address value, unused memory address value, and the remapped address value correspond to individual memory pages.

6. (Currently amended) The method of claim ~~2~~1, wherein the bad memory address value and the unused memory address value each correspond to multiple memory pages.

7. (Cancelled)

8. (Cancelled)

9. (Currently amended) The method of claim ~~2~~1, wherein the bad memory address value and the unused memory address value are exclusively-ORed to produce the remapping value.

10. (Original) The method of claim 1, wherein the remapping value and the intended address value are exclusively-ORed to produce the remapped address value.

11. (Currently amended) The method of claim ~~2~~1, wherein the bad memory address value and the unused memory address value are exclusively-NORed to produce the remapping value.

12. (Original) The method of claim 1, wherein the remapping value and the intended address value are exclusively-NORed to produce the remapped address value.

13. (Original) The method of claim 1, wherein the remapping value is latched.

14. (Currently amended) A system for remapping locations in memory, comprising:

a first logic for outputting a remapping value by combining a bad memory address value with an unused memory address value;

a second logic configured to combine the remapping value with an intended address value to generate a remapped address value, wherein one or more bad address values exist and wherein the second logic combines the remapping value with only the

intended address value that equals one of the bad memory address values to generate a remapped address value for only the one or more bad memory address values; and

a memory address input configured to access a memory location having the remapped address value.

15. (Cancelled)

16. (Currently amended) The system of claim ~~15~~14, wherein the bad memory address value, unused memory address value, and the remapped address value correspond to individual data locations.

17. (Currently amended) The system of claim ~~15~~14, wherein the bad memory address value and the unused memory address value each correspond to multiple data locations.

18. (Currently amended) The system of claim ~~15~~14, wherein the bad memory address value, unused memory address value, and the remapped address value correspond to individual memory pages.

19. (Currently amended) The system of claim ~~15~~14, wherein the bad memory address value and the unused memory address value each correspond to multiple memory pages.

20. (Cancelled)

21. (Cancelled)

22. (Currently amended) The system of claim ~~15~~14, wherein the first logic is an exclusive OR gate.

23. (Original) The system of claim 14, wherein the second logic is an exclusive OR gate.

24. (Currently amended) The system of claim ~~15~~14, wherein the first logic is an exclusive NOR gate.

25. (Original) The system of claim 14, wherein the second logic is an exclusive NOR gate.

26. (Original) The system of claim 14, further comprising a latch configured to store the remapping value.